

REMARKS

The examiner has rejected claims 1 and 16-17 under 35U.S.C. 112, first paragraph, as failing to comply with the written description requirement and enablement requirement. The examiner states that “without running a confidence check” found in the Summary of the Invention is not enough support the claim. It clearly states this in the Summary of the Invention and the summary is part of the specification. Since applicant’s claims are not dependent on such language for novelty applicants are amending the claims to remove the language to limit the issues on appeal.

The examiner rejects claims 18-20 because of the recitation of “including fast on-chip memory” does not comply with the written description or enablement requirement. Both Fig. 1 (prior art) and Fig5A reference processor 116 which refers to the same type of target processor 116. The specification makes it clear that we are describing a linker that allows other software programs or program components to build an executable program for an embedded processor having multiple memory types (page 13, lines 19-22). The specification also states that “unlike general purpose processors having a single, large memory, embedded processors have many different memories.” It continues to state that the layout of the application into various target memories impacts performance and that “certain kinds of fast on-chip memory, are limited in space and desired for critical applications” (page 10, lines 13-23). Figures 1 and 5A shows the processor 116. The specification on page 19, lines 19 and 20 refers to the visual linker providing a hierarchical, visual tree view of the target memories within the processor 116. Page 18, lines 18-19 refers to the processor 116 having embedded memories. Clearly the claims contain subject matter which is described in the specification.

The present invention relates to an improvement of a linker linking to a processor 116 with different memories including the on-chip memory as discussed on page 10. The improvement is described in detail and sufficient amount of the old structure including the processor 116 is presented in Fig. 5A. The drawing therefore adequately illustrates the application under 37 C.F.R. 83(b). If the examiner persists in this rejection applicant requests Figures 1 and 5A be labeled so that in addition to the word “Processor” for reference 116 it also calls for “DSP Processor with different memories including fast on Chip memory.” Approval for these drawing corrections if deemed necessary is respectfully requested.

In view of the above the rejections as to 35 U.S.C. 112 are overcome.

It is respectfully requested that these amendments be entered to reduce the issues on appeal.

Applicants claim 1-6, 8-9, and 12-20 are rejected under 3U.S.C. 103 (a) as being unpatentable over Lawrence in view of Mc Lain.

Known linkers report errors and may fail to complete the allocation of ingredients object files if there are unresolved symbolic references. The user then re-edits to improve or adjust the linking instructions. This activity inhibits interactive allocation strategies in which a user attempts to optimize the allocation of only a part of the ingredients of the software program before the remaining parts are available or written. No links may be left incomplete. Therefore, extensive experimentation is prohibited and users are discouraged from finding more optimal ways of linking. Known linkers are unable to resolve incomplete links. All sections must fit in memories before an output file may be created or the symbol references resolved. Unlike general purpose processor having a single, large memory, embedded processors have many different memories. The layout of the particular application into different target memories impacts performance. Certain kinds of fast memory, such as on-chip memory, are limited in space and desired for critical application functions. Trade-offs is made depending on the size of the programmer's application plus any third party components and libraries. As the program evolves and grows, the allocation decisions are revised in a time consuming manner. It is desirable to provide a system that allows a user, software program or component via command commands, gestures, and application programming interfaces to specify a link in an incomplete fashion. During such incremental specification, the link may be incomplete. The ingredient object files need not be complete and not all sections from each object file need not be placed or allocated into memory. The symbolic references need not be resolved. It is desirable to have a linker that communicates visually to the user without producing the errors or other procedures to prevent

further linking operations. The feedback desired is the allocated position and size of the sections that are allocated to memory, the values of the symbols that are allocated, a list of symbolic references that are not defined, a list of ingredient object files and sections that are not allocated. The user receives real-time on the results of the linking operations even if not all files and sections are allocated to a location in memory. The user may therefore experiment with different linking strategies without the need for actually completing the link.

Claims 1-9, 12 and 13 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Lawrence et al. (U.S. Patent No. 5,519,866; hereinafter Lawrence) further in view of McLain, Jr. (U.S. Patent No. 5,956,513; hereinafter McLain).

Response to Examiner's Response

The examiner's response to applicant's previous amendment is that Lawrence is relied upon to show "an allocation module for allocating code into different target memories of a processor without running a confidence check." The examiner recites the Abstract and col. 9, lines 60 to col.10, line 20. Nowhere is different target memories mentioned in the recited passage. Applicant has explained on page 2 of applicants' specification that DSP's have a plurality of memory types with different sizes, speeds and other characteristics. On page 6 and in Figure 3 the separate memories 312 and 314 have different locations and addresses. It is not seen where any such different target memories is mentioned in the cited passage of Lawrence. On page 19 of applicant's specification it states the linker 501 provides a hierarchical visual tree view of the target memories within the processor.

The Lawrence does not teach what the examiner states it does and does not support the claimed subject matter.

The examiner recites that Mc Lain is relied upon for “an incomplete link module, wherein said incomplete link comprises allocation information on those sections that are allocated by said allocation module and those that have not yet been allocated without running a confidence check and without actually completing the link; said allocation information including the allocated position and size of those sections that are allocated to said different target memories.” The examiner cites col. 13, lines 13-41. What applicants’ claim here is that allocation information refers to allocated position and size of those sections that are allocated to the different target memories. The referenced text of McLain refers to the ABC checking the syntax or the structure of the statement of the computer language. The user in McLain is only informed of syntax errors in the commands. It does not refer to the position and size of those sections that are allocated to the different target memories as described and claimed by the applicant. The unresolved conflicts in step 214 of Mc Lain refers only to the syntax commands. The McLain patent gives an example on col. 13, lines 21-26 about a program having many lines of code and being informed of syntax errors. It further states that the user can opt to proceed or terminate the software build and report the results. The McLain reference does not therefore teach applicants claimed invention of allocation information including the allocated position and size of those sections that are allocated to the different target memories and no combination of McLain with Lawrence teaches or suggest applicants claimed invention. Claim 1 is therefore deemed allowable over these references. Applicant’s claimed invention in amended claim 1 also calls for and “an incomplete link module, wherein said incomplete link comprises allocation information on those sections that are allocated by said allocation module and those that have not yet been allocated without actually completing the link; said allocation information including the

allocated position and size of those sections that are allocated to said different target memories.”

This is not taught by the references.

Claims 16 and 17 dependent on claim 1 are deemed allowable for at least the same reasons as claim 1. Claim 16, as amended, further calls for “said link server and a link recipe store linking instructions received that describe how the visual linker is to be controlled and can be replayed without interaction to obtain the same effect as the gestures.” The examiner in rejecting claim 16 references Col. 3 lines 45-58 and col. 9, lines 41-57 of Lawrence. There is no suggestion in this in the referenced text or seen elsewhere in Lawrence of storing linking instructions received that describe how the linker is controlled and so that it can be replayed without interaction to obtain the same effect as the gestures. There is a description of an editor capable of cutting, changing and deleting components but that is as far as it goes. There is a description of storing the components that provide for the model for the computer program but that has nothing to do with the linking instructions that describe how the visual linker is to be controlled or any suggestion of storing such link instructions so that they can be replayed without interaction. Claim 17 further calls for “said stored linking instruction are displayed and altered through said graphical user interface.” This is not taught or suggested in any the cited references. The examiner refers to any changes to the project ... are automatically saved. There is no suggestion that the linking instructions are saved. Nothing in Fig. 12 of the reference points to linking instructions.

Claim 2 calls for “recording linking instructions received that describe how the visual linker is to be controlled and so that said linking instructions can be replayed without interaction to obtain the same linking effect”. It is not seen where there is any teaching or suggestion of this in Lawrence or McLain as discussed above in connection with claim 16. Claim 2 includes the

limitation of cancelled claim 7. The examiner in rejecting claim 7 references Fig. 12 and Col. 19 lines 59-65 of Lawrence and in particular to the statement that any changes made to the Project while in the browser is automatically saved. There is no teaching or suggestion in Lawrence of recording linking instructions that describe how the visual linker is to be controlled or any suggestion of storing so the instruction may be replayed without interaction. It is not seen where McLain suggests this either. Claim 2 is therefore deemed allowable over the references.

Claim 2 calls for different subject matter than claim 1 and yet the examiner handles them as one in a confusing manner. Claim 2 calls for “generate a specific allocation instruction from a client program or program component; executing said instruction by making alterations to allocation information associated with one or more code or data sections; resolving allocation to the full extent possible given current allocation information associated with all code and data sections involved in a link; recording linking instructions received that describe how the visual linker is to be controlled and so that said linking instructions can be replayed without interaction to obtain the same linking effect; report to client programs current allocation state inclusive of allocation errors and sections not yet allocated ;and repeating these steps until all sections of code and data have been allocated.”

The examiner has referenced text in Lawrence but the references do not teach what applicant claims.

The examiner references Fig. 2, ref 212 and 214; col. 12, lines 56-60. As mentioned previously they do not teach what applicant claims in Claim 1 or for that matter what is in claim 2. The examiner also references col.13, lines 13-21. The examiner argues that this supports reporting to client programs the current allocation errors and section not yet assigned. This is not what is claimed in claims 1 or 2. The reference has nothing to do with “recording linking instructions received that describe how the visual linker is to be controlled and so that said

linking instructions can be replayed without interaction to obtain the same linking effect; report to client programs current allocation state inclusive of allocation errors and sections not yet allocated.” The examiner does not reference anything to suggest this.

Claims 3 through 6 and 8 through 13 dependent on claim 2 are deemed allowable for at least the same reasons as Claim 2. Claim 8 further calls for “the record of link instructions may be displayed and altered through a graphical user interface.” This is not taught in the references.

Claim 15, as amended, is dependent on claim 2 is deemed allowable for at least the same reasons as claim 2. Claim 15 further calls for the steps of displaying the record of the link instructions and altering through a graphical user interface. It is not seen where this is taught or suggested in the references.

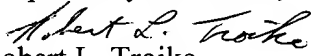
Claim 18 calls for “an allocation module for allocating sections of code and data into different target memories of a processor including fast on-chip memory” and “an incomplete link module, wherein said incomplete link comprises allocation information on those sections that are allocated by said allocation module and those that have not yet been allocated without actually completing the link; said allocation information including the allocated position and size of those sections that are allocated to said different target memories including fast on-chip memory.” As pointed out previous it is not seen where this is taught or suggested in the references. The examiner references paragraph 29 but has not presented teaching in the prior art other than related to claims 1 and 16-17 to reject the claim.

In the rejection of claims 10 and 11 Draves (U.S. Patent no. 5,950,221) is cited. It is not seen where Draves teaches what is missing in Lawrence and Mc Lain. Further, Draves is concerned with a computer system and not a linker or a linking process.

In view of the above applicants' Claims 1-6 and 8-13 and 15-20 are deemed allowable over these references and an early notice of allowance is deemed in order and is respectfully requested.

If the examiner persists in the rejection of the claims applicant respectfully requests that the amendments be entered for purposes of appeal so that the issues on appeal will be reduced.

Respectfully submitted,


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